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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/651,924	08/31/2000	Michael S Bertone	1662-31400 (P00-3212)	4257

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EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/651,924	BERTONE ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 24 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 21-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ben-Michael et al. [US Patent No 6,078,565].

4. As per claim 21, Ben-Michael discloses the invention substantially as claimed including a system, comprising:

a plurality of resources [12-18, Figure 1]; and

a receiver adapted to receive requests from said sources [26-29, Figure 1], the receiver comprising a controller [745, Figure 7; and col 6, lines 10-12] that permits said sources to provide memory requests to said receiver based on credits issued by said receiver to said sources [col 1, lines 53-62], and that automatically issues a credit to a source without the source having to request a credit [i.e. return immediately] [col 4, lines 24-26; and col 6, lines 53-55].

5. As per claim 22, Ben-Michael discloses each credit corresponds to a single request [col 1, lines 55-56].

6. As per claim 23, Ben-Michael discloses a buffer adapted to receive a plurality of requests from said sources, and said credits are issued to said sources to permit said sources to provide said requests to said buffer [i.e. plurality of virtual circuits] [col 10, lines 30-38].

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu [US Patent No 6,715,008], in view of Deneroff et al. [US Patent No 6,751,698].

9. As per claim 1, Shimizu discloses the invention substantially as claimed including a multi-processor computer system, comprising:

a plurality of processors [Figures 1 and 2], each processor coupled to at least one memory cache [204, Figure 2]; and one interprocessor router [220, Figure 2; and col 3, lines 25-48]; and

a memory coupled to each processor [206, Figure 4], each memory managed by a memory controller configured to accept memory requests from the plurality of processors [356, Figure 4]; and

wherein wherein memory requests from other processors are delivered to the memory controller by the interprocessor router [Figure 4; and col 3, lines 66-67] and wherein the memory controller allocates the memory requests from the plurality of processors in a shared buffer using a credit-based allocation scheme [Figure 4; and col 5, lines 1-7 and lines 28-38].

Shimizu does not specifically disclose

one cache control unit, and

wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit.

Deneroff discloses

one cache control unit, and wherein the memory requests from a local processor are delivered to the memory controller by the cache control unit [i.e. directory controller provides cache functions] [col 2, lines 32-40].

It would have been to a person skill in the art at the time the invention was made to combine the teaching of Shimizu and Deneroff because Deneroff's teaching of cache would allow to reduce communication overhead and increase system performance.

10. Claims 2-20 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shimizu [US Patent No 6,715,008], in view of Deneroff et al. [US Patent No 6,751,698], and further in view of Ben-Michael et al. [US Patent No 6,078,565].

11. As per claim 2, Shimizu discloses wherein:

the interprocessor router are each assigned a number of credits [col 5, lines 56-57];

at least one of said credits must be delivered by the interprocessor router to the memory controller when a memory request is delivered by the interprocessor router to the memory controller [col 5, lines 19-27].

Deneroff discloses

the cache control unit are each assigned a number of credits [col 42, lines 29-32];

at least one of said credits must be delivered by the cache control unit to the memory controller when a memory request is delivered by the cache control unit to the memory controller [col 42, lines 38-67].

Shimizu and Deneroff do not specifically disclose

wherein if the number of filled spaces in the shared buffer is below a threshold, the buffer return the credits to the source from which the credit and memory request arrived.

Ben-Michael discloses

wherein if the number of filled spaces in the shared buffer is below a threshold, the buffer return the credits to the source from which the credit and memory request arrived [col 4, lines 23-28; and col 7, lines 65-col 8, lines 14].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shimizu, Deneroff and Ben-Michael because Ben-Michael's teaching would allow to manage buffer and control the flow to prevent congestion.

12. As per claim 3, Ben-Michael discloses wherein:

wherein if the number of filled spaces in the shared buffer is above a threshold, the buffer holds the credits and returns a credit in a round-robin manner to a source from which a credit has been received only when a space in the shared buffer becomes free [col 1, lines 56-62; col 5, lines 54-50; and col 6, lines 55-57]; and

wherein if a source has no available credits, that source cannot deliver a memory request to the shared buffer [col 5, lines 6-26].

13. As per claim 4, Ben-Michael discloses wherein:

the number of credits assigned to the cache control unit and the interprocessor router is sufficient to enable each source to deliver an uninterrupted burst of memory requests to the

buffer without having to wait for credits to return from the buffer [Abstract; and col 5, lines 6-26].

14. As per claim 5, Shimizu discloses wherein:

the number of credits available in the cache control unit and the interprocessor router are stored and updated in counters located in the cache control unit and the interprocessor router [i.e. credit registers] [302, Figure 3; Abstract; and col 4, lines 1-5].

Shimizu and Deneroff does not specifically disclose

the number of credits spent by the cache control unit and the interprocessor router are stored and updated in counters located in the shared buffer.

Ben-Michael discloses

the number of credits spent by the cache control unit and the interprocessor router are stored and updated in counters located in the shared buffer [col 7, lines 23-24; and col 8, lines 19-26].

It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shimizu, Deneroff and Ben-Michael because Ben-Michael's teaching would allow to control the flows in a more efficient manner.

15. As per claim 6, Ben-Michael discloses wherein:

the threshold is the point when the number of free spaces available in the buffer is equal to the total number of credits assigned to the cache control unit and the interprocessor router [col 8, lines 33-37].

16. As per claim 7, it is rejected for similar reasons as stated above in claims 1 and 2. Furthermore, Shimizu does not specifically an associated memory, a request buffer in a front-end directory in-flight table, an L2 data cache; an L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller; and an interprocessor and I/O router unit configured to send request and response commands from remote processors to the memory controller. Deneroff discloses an associated memory, a request buffer in a front-end directory in-flight table, an L2 data cache; an L2 instruction and data cache control unit configured to send request and response commands from the processor to the memory controller; and an interprocessor and I/O router unit configured to send request and response commands from remote processors to the memory controller [col 2, lines 32-57; and col 47, lines 36-38]. It would have been obvious to a person skill the art at the time the invention was made to combine the teaching of Shimizu and Deneroff because Deneroff's teaching of L2 cache would provide additional level of caching to increase system performance.

17. As per claim 8, it is rejected for similar reasons as stated above in claims 2 and 3.

18. As per claim 9, Shimizu discloses wherein:

the credits are returned to the sources which have given up credits to the directory in-flight table in a random, equally probably manner [col 3, lines 50-65].

19. As per claim 10, it is rejected for similar reasons as stated above in claims 6 and 7.

20. As per claims 11 and 12, they are rejected for similar reasons as stated above in claims 5 and 7.

21. As per claim 13, it is rejected for similar reasons as stated above in claim 4.. Furthermore, Shimizu and Deneroff do not specifically disclose wherein the number of credits available to the L2 instruction and data cache control unit and interprocessor and I/O router is determined by the round trip time required to send a credit to and receive a credit from the directory in-flight table. Ben-Michael discloses wherein the number of credits available to the L2 instruction and data cache control unit and interprocessor and I/O router is determined by the round trip time required to send a credit to and receive a credit from the directory in-flight table [col 1, lines 63-col 2, lines 4]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Shimizu, Deneroff and Ben-Michael because the teaching of Ben-Michael would provide a convenient and inexpensive way to maintain a list of credits to be returned in thousands of virtual circuits, and to have fast access to the list [Ben-Michael, col 2, lines 20-33].

22. As per claim 14, it is rejected for similar reasons as stated above in claims 1-3.

23. As per claim 15, it is rejected for similar reasons as stated above in claim 9.

24. As per claim 16, Ben-Michael discloses wherein:

when the number of empty buffer spaces is smaller than the buffer threshold and a buffer space becomes empty, returning a credit in a random, statistically skewed manner to one of the sources which have spent credits held by the buffer [col 5, lines 44-50].

25. As per claim 17, Ben-Michael discloses

assigning a minimum number of credits to each source that is sufficient to allow each source to send a continuous sequence of data packets without waiting for returned credits [i.e. continuous burst] [col 3, lines 49-60].

26. As per claim 18, it is rejected for similar reasons as stated above in claim 3.

27. As per claim 19, it is rejected for similar reasons as stated above in claim 6.

28. As per claim 20, it is rejected for similar reasons as stated above in claim 5.

29. As per claim 24, Shimizu discloses the receiver issues credits among said sources to avoid a source from having exclusive access to said receiver to the exclusion of the other sources [Abstract].

30. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

31. A shortened statutory period for response to this action is set to expire **3 (three) months and 0 (zero) days** from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 U.S.C 133, M.P.E.P 710.02, 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (703) 305-5321. The examiner can normally be reached on flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (703) 305-8498. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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